WHAT IS CLAIMED IS:

1. A thin film magnetic memory device comprising:

a plurality of memory cells each executing data storage; and

a plurality of data lines arranged according to predetermined segments of said plurality of memory cells, respectively, wherein

each of said plurality of memory cells includes:

a magnetic storage portion magnetized in a direction according to a level of stored data, and having a different electric resistance according to a magnetization direction, and

an access element electrically connected to said magnetic storage portion in series between corresponding one of said plurality of data lines and a first voltage, and turned on in at least one selected memory cell as a data read target memory cell,

said thin film magnetic memory device further comprises:

a select gate electrically connecting the data line corresponding to said selected memory cell among said plurality of data lines to an internal node; and

a data read circuit for reading said stored data of said selected memory cell, and wherein

said data read circuit includes

a constant current circuit electrically connected between a second voltage and said internal node, and supplying a constant current according to a control voltage adjustable in a nonvolatile manner according to an external input, to said internal node, and

a voltage amplification circuit generating read data according to a voltages of said internal node.

2. The thin film magnetic memory device according to claim 1, wherein

said constant current circuit includes:

a current source circuit outputting said constant current according to said control voltage;

a first voltage terminal receiving an input of an external adjustment voltage during an operation test;

a voltage switch portion transmitting said adjustment voltage to said current source circuit as said control voltage during said operation test; and

a current monitor portion detecting said constant current during said operation test, and wherein

said current monitor portion includes

a monitor resistor portion electrically connected between said internal node and said first voltage during said operation test, and

a second voltage terminal allowing, from outside, application of a predetermined voltage and measurement of resulting current flow during said operation test.

3. The thin film magnetic memory device according to claim 2, wherein

said monitor resistor portion includes a plurality of magneto-resistance elements connected in series between said internal node and said first voltage, and each manufactured in a same manner as said magnetic storage portion.

4. The thin film magnetic memory device according to claim 1, wherein

said constant current circuit includes a voltage adjustment circuit generating said control voltage, and

said voltage adjustment circuit includes

a plurality of program elements each changing from a first state to a second state in a nonvolatile manner according to said external input, and

a voltage adjustment portion setting a voltage level of said control voltage according to a combination of the respective states of said plurality of program elements.

5. The thin film magnetic memory device according to claim 4, wherein

said voltage adjustment circuit includes,

a plurality of test gate circuits each provided to correspond to at least one of said plurality of program elements, and

a plurality of test terminals provided to correspond to said plurality of test gate circuits, and receiving external pseudo-program signals, respectively, and wherein

each of said plurality of test gate circuits is electrically connected to corresponding one of said plurality of program elements in series or in parallel, and forms a same electrical connection state as said second state of the corresponding program element, in response to a corresponding one of said pseudo-program signals.

6. A thin film magnetic memory device comprising:

a plurality of memory cells each executing data storage; and

a plurality of data lines arranged according to predetermined segments of said plurality of memory cells, respectively, wherein

each of said plurality of memory cells includes

a magnetic storage portion having one of first and second electric resistances according to a level of stored data, and

an access element electrically connected to said magnetic storage portion in series between corresponding one of said plurality of data lines and a first voltage, and selectively turned on,

said thin film magnetic memory device further comprises:

a current supply circuit supplying a current passing through said magnetic storage portion, said current supply circuit supplying a first constant current to at least one of said plurality of data lines in a normal operation mode, and supplying a second constant current higher than said first constant current, to at least one of said plurality of data lines in another operation mode.

7. The thin film magnetic memory device according to claim 6, wherein

said magnetic storage portion includes

a first magnetic body layer magnetized in a fixed direction;

a second magnetic body layer magnetized in a direction according to the level of said stored data, and

an insulating film formed between said first and second magnetic body layers, and wherein

said another operation mode corresponds to a defect acceleration test for screening said insulating film.

8. The thin film magnetic memory device according to claim 6, wherein

in the plurality of memory cells in which said access element is turned on, a bias voltage applied to both ends of said insulating film in said another operation mode is greater than the bias voltage in said normal operation mode.

9. The thin film magnetic memory device according to claim 6, wherein

said access element has a field effect transistor connected to said magnetic storage portion in series; and

in the plurality of memory cells in which said access element is turned on, a voltage applied to a gate of said field effect transistor in said another operation mode is set so that an ON-resistance of said field effect transistor is lower than the ON-resistance in said normal operation mode.

10. The thin film magnetic memory device according to claim 6, wherein

said plurality of memory cells are arranged in a matrix;

said plurality of data lines are arranged to correspond to respective memory cell columns;

said thin film magnetic memory device further comprises a plurality of select gate circuits provided corresponding to respective memory cell columns, and controlling connection between said current supply circuit and said plurality of data lines; and

each of said select gate circuits connects N data lines (N: an integer not less than 2) among said plurality of data lines to said current supply circuit in said another operation mode, and connects one data line among said plurality of data lines corresponding to a selected memory cell, among the plurality of memory cells, as a data read target memory cell.

11. The thin film magnetic memory device according to claim 6, wherein

said plurality of memory cells are arranged in a matrix;

said thin film magnetic memory device further comprises a row select portion controlling said access element to be turned on and off for each memory cell row; and

said row select portion turns on access element groups corresponding to M memory cell rows (M: an integer not less than 2) in said another operation mode, and turns on the access element groups corresponding to one memory cell row corresponding to a selected memory cell, among the memory cells, as a data read target memory cell in said normal operation mode.

12. The thin film magnetic memory device according to claim 6, wherein

said current supply circuit includes

a current source circuit for outputting a constant current according to a control voltage to the at least one of said data lines in each of said normal operation mode and said another operation mode,

a first voltage adjustment circuit adjusting a first reference voltage corresponding to said first constant current;

a second voltage adjustment circuit adjusting a second reference voltage corresponding to said second constant current; and

a voltage switch circuit transmitting one of said first and second reference voltages to said current source circuit as said control voltage in accordance with an operation mode.

13. The thin film magnetic memory device according to claim 12, wherein

said first voltage adjustment circuit adjusts said first reference voltage in a nonvolatile manner in response to a first external input; and

said second voltage adjustment circuit adjusts said second reference voltage in a nonvolatile manner in response to a second external input.

14. The thin film magnetic memory device according to claim 12, wherein

said first voltage adjustment circuit adjusts said first reference voltage in a nonvolatile manner in response to a first external input; and

said second voltage adjustment circuit generates said second reference voltage according to said first reference voltage from said first voltage adjustment circuit so that a ratio of said first reference voltage to said second reference voltage has a predetermined value.

15. The thin film magnetic memory device according to claim 6, further comprising

a dummy memory cell provided for M memory cells (M: an integer not less than 2) among said plurality of memory cells, wherein

said dummy memory cell includes

a dummy magnetic storage portion having an intermediate electric resistance between said first and second electric resistances, and

a dummy access element electrically connected to said dummy magnetic storage portion in series between one of said plurality of data lines and said first voltage, and selectively turned on, and wherein

a current stress applied to said dummy magnetic storage portion in said another operation mode is higher than a current stress applied to said magnetic storage portion in at least one test target memory cell among said plurality of memory cells.

16. The thin film magnetic memory device according to claim 15, further comprising

a driver circuit controlling said access element and said dummy access element to be turned on and off, wherein

said driver circuit sets a product of time for which a third constant current passes through said dummy magnetic storage portion and said third constant current, to be M times as large as a product of time for which said second constant current passes through said magnetic storage portion of said test target memory cell and said second constant current.

17. The thin film magnetic memory device according to claim 15, wherein

each of said access element is constituted of a first field effect transistor, and each said dummy access element is constituted of and a second field effect transistor,

said thin film magnetic memory device further comprises a driver circuit controlling said access element and said dummy access element to be turned on and off, and

said driver circuit sets each of gate voltages of said first field effect transistor and said second field effect transistor included in said at least one test target memory cell among said plurality of memory cells so that an ON-resistance of said second field effect transistor is lower than an ON-resistance of said first field effect transistor in said another operation mode.

18. The thin film magnetic memory device according to claim 15, further comprising

a driver circuit controlling said access element and said dummy access element to be turned on and off, wherein

said driver circuit sets an on-period of said dummy access element to be longer than an on-period of said access element in said at least one test target memory cell.

19. The thin film magnetic memory device according to claim 6, wherein

said current supply circuit includes

a read drive portion connecting the at least one data line to a second voltage higher than said first voltage, and

a data write circuit operating by being supplied with a third voltage higher than said second voltage, and generating a data write current magnetizing said magnetic storage portion of a selected memory cell, among said plurality of memory cells, as a data write target memory cell in accordance with the level of the stored data during data write in said normal operation mode,

said thin film magnetic memory device further comprises a select gate circuit controlling connection between said current supply circuit and said plurality of data lines;

said select gate circuit connects one of said read drive portion and said data write circuit to the at least one corresponding data line among said plurality of data lines corresponding to said selected memory cell in said normal operation mode, and connects said data write circuit to the at least one data line among said plurality of data lines, corresponding to test target memory cells in said another operation mode, and wherein

said data write circuit supplies said second constant current in said another operation mode.